Doc Code: AP.PRE.REQ

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 03226/037001; P5009

	Application Number 09/778,424-Conf. #6879	Filed February 7, 2001
	First Named Inventor Joseph C.H. Park	
	Art Unit 2193	Examiner T. A. Vu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
    Note: No more than five (5) pages may be provided.

I am the

[ ] applicant /inventor.

[ ] assignee of record of the entire interest.
    See 37 CFR 3.71. Statement under 37 CFR 3.73(b)
    is enclosed. (Form PTO/SB/96)

[x] attorney or agent of record.
    Registration number   45,079

[ ] attorney or agent acting under 37 CFR 1.34.
    Registration number if acting under 37 CFR 1.34. _____

_____
Signature

Thomas K. Scherer
Typed or printed name

(713) 228-8600
Telephone number

March 17, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

[ ] *Total of ___1___ forms are submitted.

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Docket No.: 03226/037001
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Joseph C. H. Park

Conf. No.: 6879

Application No.: 09/778,424

Art Unit: 2193

Filed: February 7, 2001

Examiner: T. A. Vu

For: GENERAL AND EFFICIENT METHOD FOR
        TRANSFORMING PREDICATED
        EXECUTION TO STATIC SPECULATION

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1, 3-6, 10, 12-15, and 17 stand rejected under 35 U.S.C. §103(a) as being obvious over Intel® IA-64 "Architecture Software Developer's Manual (hereinafter "IA-64") in view of "A Framework for Balancing Control Flow and Predication" by Hwu et al. (hereinafter "Hwu"), further in view of U.S. Patent No. 6,637,026 issued to Chen (hereinafter "Chen").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (See MPEP §2143).

In maintaining the above rejection and issuing a final office action, the Applicant respectfully asserts that the Examiner has failed to satisfy the requirements set out in MPEP §2143, which require that the cited prior art teach or suggest all claim limitations.

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In particular, the Applicant respectfully asserts that the Examiner, in construing the claims, has failed to consider the claim limitations in their entirety.

Turning to the claims, the claims require if-converting an abstract internal representation, wherein the if-converting comprises, in part, writing Boolean data to a general register designated as a destination register based on the testing, the destination register corresponding to the conditional instruction and representing a predicate. The above limitation is addressed below.

As asserted in the Advisory Action mailed March 13, 2006, as well as in the Office Actions mailed April 21, 2005, and October 17, 2005, the Examiner has broadly interpreted the teachings of IA-64 to read on the pending claims. In particular, the Examiner has construed the teachings of IA-64, which is directed to software development for a particular processor architecture, to cover writing Boolean data to a general register designated as a destination register, the destination register corresponding to the conditional instruction and representing a predicate (*i.e.*, the Examiner asserts that using a general register to store predicate Boolean data is equivalent to designating a generic register, which, in effect, makes it a predicate register) (see Office Action dated October 17, 2005, at page 10; continuation sheet of Advisory Action mailed March 13, 2006).

The Applicant respectfully asserts that the broad interpretation of IA-64 is overreaching and has effectively removed explicitly stated limitations within the claims. In particular, the Examiner has construed teachings in IA-64 directed to storing predicates in specialized predicate registers (see Office Action dated October 17, 2005, at page 10) to be equivalent to the limitation that the if-converting comprises "writing Boolean data to a general register designated as a destination register based on the testing, the destination register corresponding to the conditional instruction and representing a predicate." As

previously discussed in the Response to final Office Action mailed to the U.S. Patent Office

on January 13, 2006, pp. 3-4, such an interpretation effectively reads out the limitation that

Boolean data is written to a *general* register designated as a destination register. The use of a

specialized predicate register is not equivalent to the use of a general register, and, in

construing the claims, the Examiner has read out this limitation.

Conclusion

In view of the above, Applicant believes that the Examiner has failed to satisfy

the requirements set forth in MPEP §2143 to establish a rejection under 35 U.S.C. §103.

Accordingly, a favorable decision from the panel is respectfully requested. Please apply any

charges not covered, or any credits, to Deposit Account 50-0591 (Reference

Number 03226/037001).

Dated: March 17, 2006   Respectfully submitted,

By_____
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